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Patentanmeldung Nr. Patent application No. Demande de brevet n°

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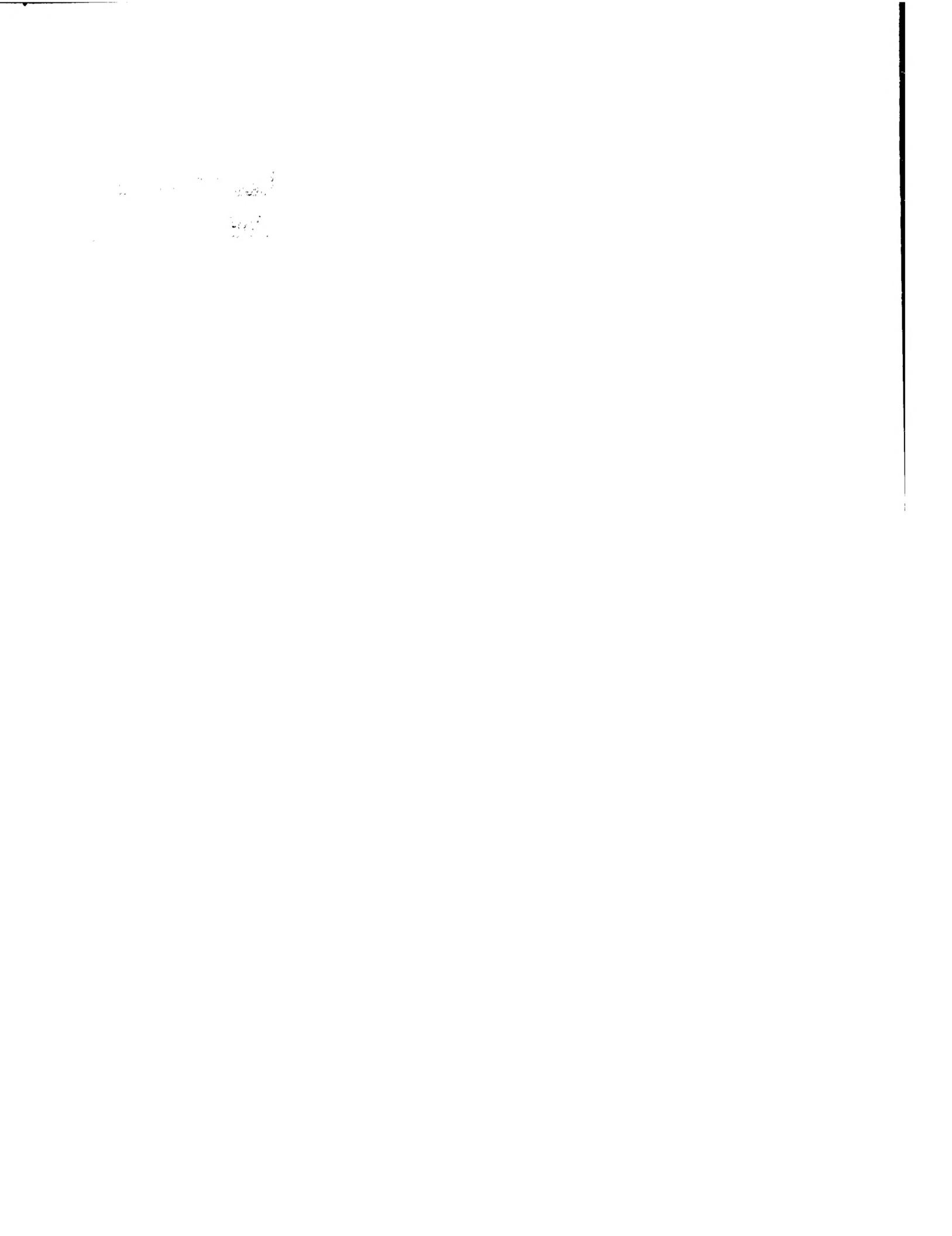
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Bezeichnung der Erfindung/Title of the invention/Titre de l'invention:
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Method of testing PLL and module including a PLL

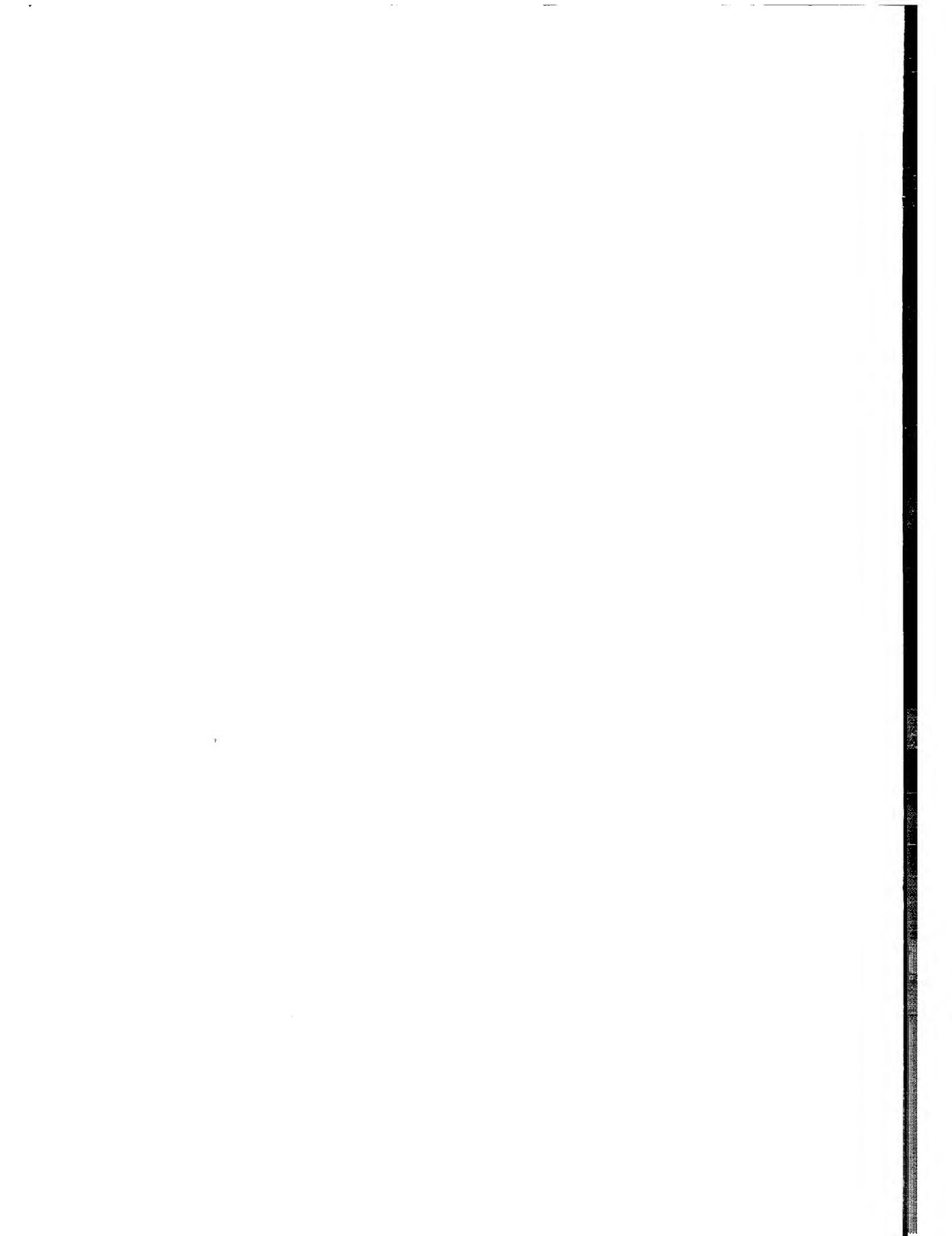
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Method of testing a PLL and module including a PLL

The present invention relates to method of testing a PLL and PLL including a test device.

PLL systems are traditionally tested using functional specifications, where the functionality of the circuit is verified at some pre-specified test points. A complete functional test includes measuring several parameters, such as locking time, locking-frequency range, capture-frequency range, and jitter transfer function. However, measuring all PLL's relevant parameters would incur a very high cost; complete functional testing of an integrated PLL is economically impractical for production stage testing. Thus, manufacturers usually perform only a selected number of tests. In particular, the frequency lock test is one of the most widely used. It verifies a PLL's primary functionality by observing its output frequency in the locked state for a given reference input frequency. Manufacturers can implement this test by measuring the output frequency directly with a time interval analyser or by using algorithmic techniques on strobed output clocks. However, this type of frequency measurement suffers from low throughput and usually requires specific test equipment to achieve accurate results. In addition, it requires the PLL to be in a locked state, which also significantly reduces test throughput. Generally digital PLL testing procedures can be reduced to multiple time measurements between two events of a waveform, followed by data processing, regardless of whether frequency, jitter or locking information is the issue of interest. However, dependent on the design, some DC tests can be carried out at the PLL too (supply current, band gap reference voltage, matching of the charge pumps). As mentioned above, the following test parameters are applicable for testing PLLs: Lock Behaviour, Center Frequency, Close Loop Test, Open Loop Test, Bit Error Rate, Jitter.

Looking for solutions, test engineers are tempted to break the task and verify sub-blocks independently. This strategy, referred to as structural testing, has been successfully applied to digital testing problems. However analog circuits are much more complex and do not lend themselves as easily to this methodology. Furthermore, the nature of the phase-locked loop renders this solution unattractive as the closed-loop feedback makes it difficult to relate the specifications from the PLL level to the block level. Test development is further hampered by the computational power required by even simple simulation of the PLL. This is due to the order of magnitude spread in the time constant of the device.

Fault-based testing is an attractive alternative to functional testing, which targets the presence of physical defects in a PLL, thus providing a quantitative measure of the test process. Studies on a number of analog circuits show that relatively simple tests can give high test coverage for common defects, and this can be achieved by using the defect-oriented testing (DOT) approach. At the same time it also became clear that these tests are not able to detect all products that are faulty due to process parametric variations.

It is a purpose of the present invention to provide a method which makes it possible to efficiently detect verify a PLL in a plurality of respects. It is a further purpose of the invention to provide a module including a PLL which has facilities for testing the PLL.

According to the method of the invention the PLL is provided with a power supply voltage having a voltage variation profile, the voltage variation profile including a relatively fast voltage rise and a relatively slow voltage decay, and wherein an output signal of the PLL is compared with a template response.

5 A module according to the invention comprises a power supply unit for providing the PLL with a substantially constant voltage during a normal operating mode and for providing the PLL with a power supply voltage having a voltage variation profile in a test mode, the voltage variation profile including a relatively fast voltage rise and a relatively slow voltage decay, the PLL including a feedback facility for in a normal operating mode providing a further signal derived from an output signal of the controlled oscillator, the feedback facility being disabled during test mode, the module further comprising a comparison unit for comparing an output signal of the PLL with a template response.

10 The output signal measured can be for example the input signal of the controlled oscillator, the output signal of the oscillator or the current delivered by the power supply to the PLL.

15 During variation of the power supply voltage of the PLL the transistors in the circuit operate in all the regions of operation, namely cut-off, weak inversion, linear and saturation, and hence, provide bias currents rich in information. The method measures current signatures, not single values. Many faults have unique or near-unique signatures, easing the diagnosis process. Indeed it is independent of the linearity or nonlinearity of the systems, circuit or component. Because the voltage variation profile includes a relatively fast voltage rise and a relatively slow voltage decay it is prevented that the controlled oscillator starts operating during test mode. In this way disturbance of the current signatures strongly reduced. During the rising portion of the voltage profile all nodes of the circuit go to their nominal values (as expected). Also, the oscillator will have the right biasing to start oscillating. By limiting the 20 time that the nodes of the oscillator are at their nominal voltage, it is possible to prevent the oscillator from running or reaching its target frequency, in other words the oscillator will not work properly.

25

It is remarked that in "Analog Fault Diagnosis Based on Ramping Power Supply Current Signature Clusters", by Shyam S. Somayajula et all., IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing, Vol. 43, No. 10, October 1996 a method is described for testing analog circuits wherein the power supply voltage is ramped. This method as described therein would not be suitable for testing PLL's, because the power supply voltage variation comprises a relatively slow voltage rise. This would cause the controlled oscillator to start oscillating during test, which on its turn would disturb the current signatures measured and could cause a false diagnosis.

30 The module comprising the PLL and the facilities for testing it may be integrated on an IC. The module may have an external input to select test mode or normal mode so that the module can be tested from time to time to verify whether it still functions correctly.

35 Alternatively the test may be carried out during the manufacturing stage. In that case the facilities for testing may be disabled after the test is completed.

40 In an embodiment the power supply voltage is maintained at a relatively constant value after the voltage rise and before the voltage decay. This voltage plateau has to be short enough to prevent the oscillator from oscillating, but large enough to initialize the nodes of the circuit

45 In a further embodiment the voltage variation profile is periodically repeated. By periodically repeating the profile a plurality current signatures can be generated. By averaging these an average profile can be obtained in which incidental variations are suppressed. In this way a more reliable diagnosis can be given of the PLL.

50 In an embodiment the repetition frequency is within the nominal operating frequency range of the PLL.

By several variations of the method different aspects of the PLL can be verified. In a first variation of the method a constant signal value is provided as the reference signal and the further signal. In this way the phase detector of the PLL is not initialized during the test. This is in particular relevant for a PLL having a digital phase detector. In this way the first stage of the PFD, usually constituted by flip-flops, is not enabled. The PFD is bypassed, so that deviations in other parts of the PLL can be measured more accurately.

In other variations of the method a periodic signal having the same frequency is provided as the reference signal and the further signal. In this way the first stage of the PFD is initialized. By applying a phase difference between the power supply voltage profile and the periodic signal the PLL can be measured under different conditions.

Favorable choices for the phase difference are values of $\pi/2$ and $3\pi/2$.

Embodiments of the present invention are described in APPENDIX 1: Power Supply Ramping for Quasi-Static Testing of PLLs" by José Pineda de Gyvez et all.

The template response of the PLL in the ideal case may be obtained from the response of a PLL of which it was already determined in an other way that it functions properly, or from a circuit simulation of a PLL. It was found that the template response, or golden response comprises a high amount of high frequency variations. Although it is possible to analyze the high frequency content and compare that with the content of the template response this may require expensive circuitry. Figure 1a of APPENDIX shows the ripples in the measured output signal, the quiescent current in this case. Figure 1b schematically shows the difference with the golden signature.

In a preferred embodiment therefore the output signal is filtered, rectified and integrated. The result of the integration can be compared with the integration result for an ideal or modelled PLL.

A module wherein the comparison unit comprises a high-pass filter HPF for filtering the output signal I_{DD} , a rectifying element D1 for rectifying the filtered output signal and an integrator C_{hold} for integrating the rectified filtered output signal is schematically shown in Figure 2 of APPENDIX II and more in detail in Figure 4 thereof.

In Figure 3 an example is shown of the test signals used when performing the test. The Ramp test signal is the voltage variation profile of the power supply, having a relatively short rise time T_{RISE} , a relatively long decay time T_{RAMP} and an intermediate hold time T_{VDD} . The integrator is periodically discharged with the signal "Switch Test Signal" during a relatively short portion of the repetition period., here 0.3 times the clock period. Rise and hold of the ramp test signal take place during the discharge activity of the integrator.

In the embodiment of Figure 4 the cut-off frequency, can be controlled with the variable capacitor C_{hpf} . In this way a spectral analysis of the current signatures can be carried out. Figure 5 shows the output signal V_{OUT} of the integrator C_{hold} for various settings of the capacitor. Figure 6 shows a more detailed view of the output signals V_{OUT} . Figure 7 shows the changes in the output signal V_{OUT} for several corner frequencies when ten different types of bridges are introduced in the PLL.

Figure 8 shows the effect on the power spectrum density. Therein the output voltage V_{OUT} of the integrator is shown as a function of the corner frequency of the high pass filter HPF for an ideal PLL (VOUT_gold) and for 10 erroneous PLLs (VOUT_1, ..., VOUT_10)

APPENDIX I

Power Supply Ramping for Quasi-static Testing of PLLs

5

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10

Abstract

An innovative approach for testing PLLs in open loop -mode is presented. The operational method consists of ramping the PLL's power supply by means of a periodic sawtooth signal. The reference and feedback inputs of the PLL in open-loop mode are connected to the clock reference signal or to ground. Then, the corresponding quiescent current, clock output, and oscillator control voltage signatures are monitored and sampled at specific times. When the power supply is swept, all transistors are forced into various regions of operation causing the sensitivity of the faults to the specific stimulus to be magnified. The developed method of structural testing for PLLs yields high fault coverage results making it a potential and attractive technique for production wafer testing.

1. Introduction

PLL systems are traditionally tested using functional specifications, where the functionality of the circuit is verified at some pre-specified test points. A complete functional test includes measuring several parameters, such as locking time, locking-frequency range, capture-frequency range, and jitter transfer function [1-5]. However, measuring all PLL's relevant parameters would incur a very high cost; complete functional testing of an integrated PLL is economically impractical for production stage testing. Thus, manufacturers usually perform only a selected number of tests. In particular, the frequency lock test is one of the most widely used. It verifies a PLL's primary functionality by observing its output frequency in the locked state for a given reference input frequency [6]. Manufacturers can implement this test by measuring the output frequency directly with a time interval analyser or by using algorithmic techniques on strobed output clocks. However, this type of frequency measurement suffers from low throughput and usually requires specific test equipment to achieve accurate results. In addition, it requires the PLL to be in a locked state, which also significantly reduces test throughput.

Generally digital PLL testing procedures can be reduced to multiple time measurements between two events of a waveform, followed by data processing, regardless of whether frequency, jitter or locking information is the issue of interest. However, dependent on the design, some DC tests can be carried out at the PLL too (supply current, band gap reference

voltage, matching of the charge pumps). As mentioned above, the following test parameters are applicable for testing PLLs: Lock Behaviour, Center Frequency, Close Loop Test, Open Loop Test, Bit Error Rate, Jitter.

5 Looking for solutions, test engineers are tempted to break the task and verify sub -blocks independently. This strategy, referred to as structural testing, has been successfully applied to digital testing problems. However analog circuits are much more complex and do not lend themselves as easily to this methodology. Furthermore, the nature of the phase-locked loop renders this solution unattractive as the closed-loop feedback makes it difficult to relate the specifications from the PLL level to the block level. Test development is further hampered by the computational power required by even simple simulation of the PLL. This is due to the order of magnitude spread in the time constant of the device.

10 Fault-based testing is an attractive alternative to functional testing, which targets the presence of physical defects in a PLL, thus providing a quantitative measure of the test process. Studies on a number of analog circuits show that relatively simple tests can give high test coverage for common defects, and this can be achieved by using the defect-oriented testing (DOT) approach [7-10]. At the same time it also became clear that these tests are not able to detect all products that are faulty due to process parametric variations. However, as result of the ever increasing functional complexity of mixed-signal ICs and the improved IC 20 fabrication-process control, spot defects are the dominant yield limiter in a mature process and a dominant cause of customer rejects for a product in high volume production.

2. Overview of Conventional PLL Testing

25 Lock behavior of a PLL can be tested by frequency or period measurements after applying certain conditions because the frequencies are stable in case of a locked PLL, or by scanning the status of the lock detector. Normally, testing a PLL, a clock signal is used as input. To determine a PLL's center frequency, edges, periods, and signal averages are commonly measured. Actually, there are two main methods for the effective frequency measurements: 30 period and frequency measurement. Measurements of the actual output frequency and also for reference frequency are quite easy to do using a time measurement instrument, measuring several period lengths of the PLL output signal and averaging the values. Another method is using the stop after n -th event function of a timer and dividing the measured time by the number of periods. The same procedure is possible using a counter and defining a fixed time interval. The accuracy depends on the window length and can be improved, so far as test time 35 constraints allow it. BER is a test strategy originally developed for testing Modulators and Demodulators, but also it can be applied on feedback closed loop systems like PLLs. BER can characterize the performance degradation of phase noise effect on digital communications. Commonly two main strategies are used for jitter measurement testing: *Testing Jitter generated by the PLL Circuit*, which is carried out without adding jitter to the reference signal, and *Jitter Transfer Function / Jitter Tolerance Testing*, in which the input 40 data stream contains a base line data rate plus an additional component of the modulated jitter. In the second case, the ATE must be able to generate a modulated stimulus with a defined modulation frequency (usually sinusoidal) and amplitude. Then the ability of the PLL to remain locked (tracking) can be tested.

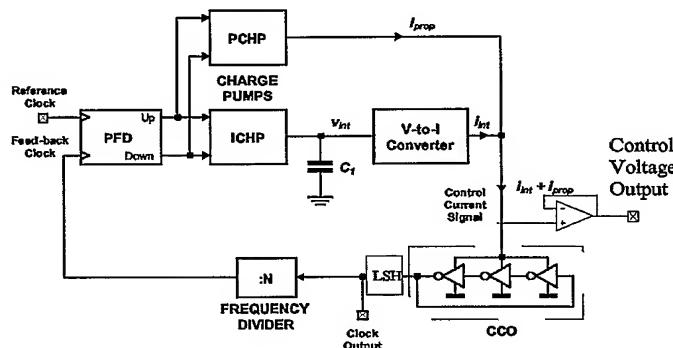
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3. The PLL under test

50 The TESTRA phase-locked loop is based on a charge pump special structure in which two separate charge pumps are used. A simplified schematic is shown in Figure 1. A standard digital phase/frequency detector controls the two charge pumps that are respectively the integral charge pump and the proportional charge pump. The second one has a role of auxiliary charge pump as will be explained later. Both charge pumps have an interaction with

the loop filter by means of the output currents I_{ICHP} and I_{PCHP} , which are applied to different nodes of the loop filter. The latter consists basically of a voltage/current converter that provides the control current signal that is essential for driving the current controlled oscillator (CCO). Capacitor C_I is the basic component for the filtering stage. The PFD control signals

5 *Up* and *Down* of the integral charge pump ICHP are switched to obtain the correct control signal corresponding to the phase error detected by the PFD. Actually, when the *Up* signal goes high the lower branch of PCHP is switched on pulling current from capacitor C_I increasing the voltage between its limit values. Conversely, when the *Down* signal goes high the up branch of ICHP is switched on pushing current into capacitor C_I and decreasing the voltage between its limit values. A voltage-to-current converter is essential on this stage to force the control current signal into the oscillator. The oscillator is current controlled based and consists essentially of a ring structure. A level shifter LSH is following to the CCO. Its purpose is to bring voltage swing of the clock output signal between the range of 3 Vpp and to set the duty cycle at 50%. A frequency feedback divider with division factor 32 closes the loop of the PLL. Finally, an op-amp buffer provides the control voltage for the next stage. According to the reference frequency that ranges from 9.84 MHz to 13.56 MHz, the output clock signal can cover a frequency from 315 MHz to 434 MHz with a division factor of 32 (or 630 MHz to 868 MHz with a division factor of 64).



20

Figure 1. Block diagram of PLL under test

4. VDD Ramp Test Methodology

The supply current monitoring technique has found no practical widespread application in 25 analog circuits. This is mainly because analog faulty behaviours are not so pronounced as those in the digital case; special test vectors often have to be applied to increase fault coverage, in a special test mode [11]. To apply the power supply current observation concept to analog fault diagnosis, major modifications should be made to the existing current testing techniques. This is because of two factors:

30 • The method requires more than a simple observation of abnormal currents;
 • Unlike digital circuits, bias currents always exist between the power supplies in analog circuits and in most cases abnormal currents cannot be defined.

35 For analogue circuits and systems, fault diagnosis techniques are more complex when compared to their counter parts in digital circuits for various reasons:

- The requirement of measurements of current and voltage signals at the internal nodes;
- Diagnosis errors caused by soft-faults which are due to the tolerance of the components.

An advanced methodology for testing analog circuits based on the observation of power supply currents was proposed in the late 90s [12]. To obtain signatures rich in information for efficient testing, the transistors in the circuit are forced to operate in all possible regions of operation by using a ramp signal at the supply instead of the conventional constant DC signal or ground voltage.

The power supply ramping technique can potentially detect and diagnose single and multiple shorts as well as open circuits. The application of a ramp signal at the power supply nodes instead of the conventional step (or DC voltage) can potentially make the majority of the transistors in the circuit operate in all the regions of operation, namely cut-off, weak inversion, linear and saturation, and hence, provide bias currents rich in information. The method measures current signatures, not single values. Many faults have unique or near-unique signatures, easing the diagnosis process. Indeed it is independent of the linearity or nonlinearity of the systems, circuit or component.

15

5. Quasi-static PLL Testing Methodology

Figure 2 illustrates the basic test strategy. The circuit under test (PLL in open-loop mode) is excited with a transient test stimulus provided to the power supply input and the circuit response is sampled at specified times to detect the presence of a fault. The power supply transient waveform (test pattern) is formed from piecewise linear segments in order to excite the circuit so that the sensitivity of the fault to the specific stimulus is magnified. The used waveform consists of a periodic sawtooth signal with a narrow rise time (fast positive ramp) and a wide rise time (slow negative ramp). The power supply voltage is then swept between GND and nominal VDD with a frequency value within the nominal operating range of the PLL. The resulting signature outputs are evaluated by monitoring the I_{DD} power supply current, the PLL's clock output and oscillator control voltage signals. Sampling these signatures at specified times the presence of a fault can be detected. This new power supply ramp method for quasi-static testing of PLLs is explored and evaluated in this work as a structural test capable of testing PLLs in open-loop mode. The underlying testing approach relies on a defect oriented test analysis that takes into account the spread of the process as well as the presence of resistive defects.

35

The main idea is to provide a sawtooth signal to the power supply pin VDD with a steady frequency related to the nominal reference clock frequency. Therefore the I_{DD} current signature and the CCO's control output voltage, VOSC, are measured by sampling the respective signatures at different established test points. Figure 3 shows the sawtooth signal used as power supply test pattern for the open loop PLL's circuit. The sawtooth wave's rise time is set to have a sharp positive edge to initialise the digital circuitry. The width of the ramp time, is narrow enough to prevent the CCO from starting. In this way the monitored waveforms I_{DD} , VOSC and CLKOUT present no additional ripple and the sampling task for testing the PLL easily executed. There are three strategies to synchronize the V_{DD} signal with the clock inputs of the PLL. They are:

40

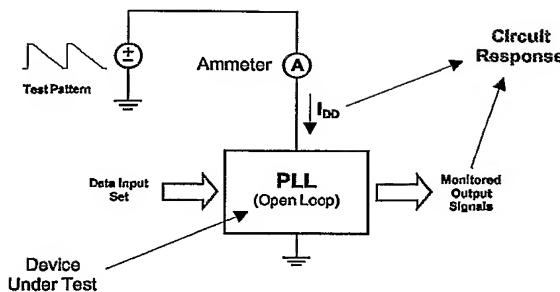


Figure 2. Quasi-static test setup strategy

5 **TEST 1-00.** The PLL's input CLKIN and CLKFB are connected to GND (grounded state). Then, the PLL's IDD power supply current, CLKOUT and VOSC output voltage are monitored on fixed test points during the time that the sawtooth signal is provided to the power supply pin VDD.

10 **TEST 4-25.** The PLL's input CLKIN and CLKFB are connected to a square wave generator and the VDD ramp test signal is delayed by 25% of the period in relation to the reference clock signal (positive edge). Then the PLL's IDD power supply current, CLKOUT and VOSC output voltage are monitored on fixed test points during the time that the sawtooth signal is provided to the power supply pin VDD.

15 **TEST 4-75.** The PLL's input CLKIN and CLKFB are connected to a square wave generator and the VDD ramp test signal is delayed by 75% of the period in relation to the reference clock signal (positive edge).

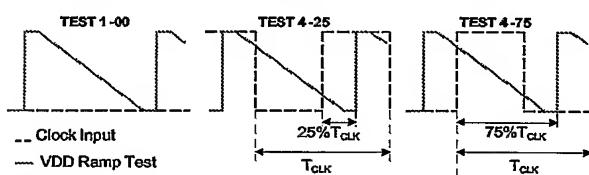
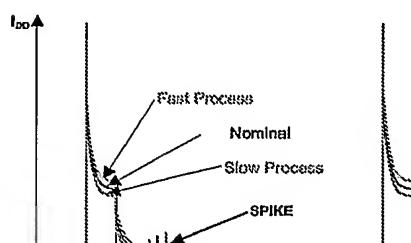


Figure 3. Syncrhonization of VDD waveform with clock input

20 Actually, the digital part of the open loop PLL is not initialized by means of TEST 1 -00. In fact the test is carried out keeping the inputs of the phase/frequency detector connected to ground. The flip -flops, which constitute the first stage of the PFD, are not enabled because no positive edge occurs at the inputs. The initialization is alternatively achieved by means of TEST 4 -25 and TEST 4-75 on which the square wave clock is provided to the PFD's inputs. The difference between the latter two tests is due to the phase shift of the ramp test signal in relation to the clock input signal. TEST 4 -25 aligns the negative edge of the clock with the negative side of the VDD ramp around a voltage value $VDD \approx 2.5$ V; TEST 4-75 makes the positive edge of the clock correspond with the negative ramp around a voltage value $VDD \approx 2.5$ V. In the first case the flip-flops of the PFD are already initialised and resetted, when the VDD ramp starts to decrease, because of the high logic state at both the inputs. In the second case both flip-flops switch to a high logic state and immediately to a low logic state due to the reset forced by the feedback NAND of the PFD.

25 **30** Notice that while IDD testing the fast process results in more current during the discharging of the circuit, while the slow process results in less current. As expected the nominal process provides a discharging current in between the mentioned fast and slow. From the previous explanation the following standard waveform displayed in Figure 4 can be considered for each test. Four main different regions can be classified for the I_{DD} current signature:



5

Main strong spike and discharge. It is the same for every test. After the spike a fast discharge of the circuit occurs during the 10% of the period on which the V DD is equal to the nominal value of 3 V. This discharge is the trend of the circuit to stabilize the power supply current to the normal value. In this part the process corners are very close to each other. Finally, a step occurs on the I_{DD} current starting to ramp down the VDD power supply voltage.

10

Positive I_{DD} discharging. I_{DD} decreases with a low slope after the step when the VDD voltage is ramped down. This region is bounded until the I_{DD} current crosses the zero value and becomes negative. Here, the process corners are more separated and different events can be distinguished for each test. The main difference is in the ripples observed because of the crossing with respect to the clock edges.

15

Negative I_{DD} discharging. This region is the most critical part of the I_{DD} signature due to the negative value of such current. Indeed, the discharging current curves cross each other to establish the same behaviour for negative current values, where the fast process generates the highest current. Furthermore, extra spikes occur for the fast process signature because of the higher amount of current through the level shifter in linear region of operation.

20

Final I_{DD} discharging. This region corresponds to the part of the VDD ramp test pattern equal to 0 V (10% of the period). The trend of I_{DD} is to discharge the circuit up to 0 mA, when a new strong positive spike occurs due to the next VDD ramp. The fast process also in this region generates more current on the circuit discharging.

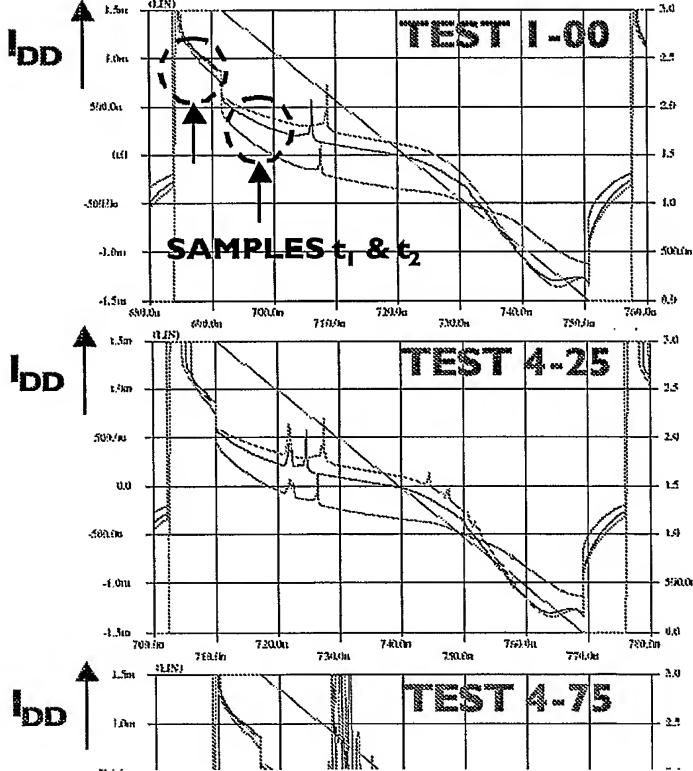
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Transient simulations for each test have been carried out with the test bench shown in Figure 5. The simulations have been executed by means of SPICE-like simulator for different process corners: *slow*, *nominal* and *fast* processes. VDD is kept at nominal values for four periods of the clock, and then the ramping of the supply is started with the conditions above reported. Output step accuracy of 20ps is used for the simulation time resolution in order not to miss high frequency ripples and extra oscillations of the monitored signals. Indeed, the CCO oscillates during the time $VDD = 3$ V and extra ripples are present on the I_{DD} signatures corresponding to the first two ramps.

30

One can explain the nature of the I_{DD} curve by looking at the RC properties of a generic network. In a RC network, the capacitor C is charged through the resistor, by the fast rising edge of the test ramp signal. This causes the strong current spike. After that, when VDD decreases, the energy stored in the capacitor is given back to the supply generator. This causes the decay of the negative current to be directly proportional to the size of the capacitor.

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20 To understand the current spikes in region -1 and region -2, we investigated the current properties of each module component of the PLL. We found that all modules present a main strong spike corresponding to the rising edge of the VDD ramp signal, that summed altogether generate the strongest spike on the global I_{DD} signature of region-1. For region-2, instead, only the level shifter and its output buffer stage cause extra spikes and ripples on the power supply current decay. This effect has its origin from the digital implementation of such functional blocks that consist of a CMOS inverter based circuitry. Indeed, decreasing the VDD power supply voltage makes the inverters work in the linear region of the voltage transfer characteristic. In such a way, both transistors pMOS and nMOS conduct for a very short time and the highest value of power current occurs in the path $VDD \rightarrow GND$ generating the regular spike on all the I_{DD} current signatures.

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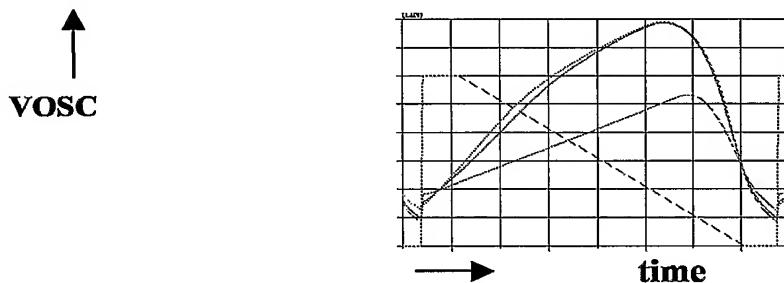


Figure 4. Control VCO signal as test signature

35 Figure 4 shows the controlling signal of the VCO. This signal can also be used for testing purposes. Two main different regions can be classified for the VOSC voltage signature.

40 **Positive slope region.** The VOSC signal grows with a positive slope from the occurrence of the VDD ramp rise edge. The highest slope corresponds to the fast process; the lowest one corresponds to the slow process, while the slope related to the nominal process is in between. The curves stop growing at around $VDD \approx 0.5 \div 0.8$ V (threshold voltage of this $0.75 \mu m$ CMOS technology). It is important to consider the point related to the flat part of the ramp pattern V where all the VOSC curves present no dependence on the process corners.

45 **Negative slope region.** The VOSC signal decreases with a negative slope from the instant on which $VDD \approx 0.7$ V. Also in this case there is a point where all the VOSC curves present no dependence on the process corners. This corresponds to the instant the ramp pattern reaches the voltage $VDD = 0$ V.

6. Loading effects on the current signature

50 Chip bonding wires introduce a parasitic inductance. The existence of this parasitic effect is one of the most difficult problems to be solved on production testing of ICs for high frequency applications. The main effect is a

resonant oscillation and strong extra ripples in the current waveform. Consequently the VDD ramp test method is affected as well. The mentioned effect can be visualized in Figure 5 for TEST 4-75.

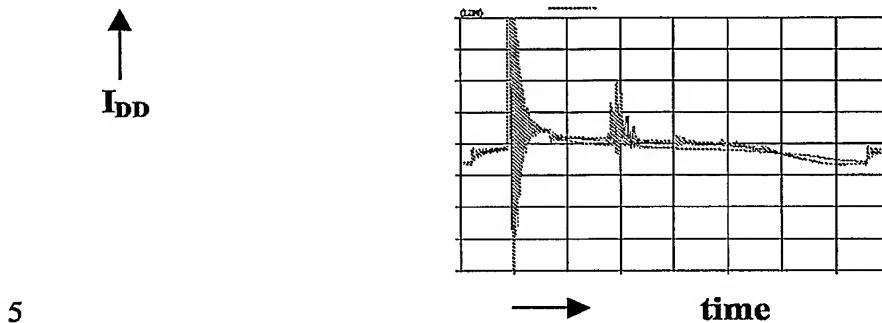


Figure 5. IDD signature with parasitics taken into account

It is really evident that for the presence of strong ripples no measurable test sample can be considered reliable, especially in the regions of interest. Therefore, an improvement on the test bench has been developed by use of a low-pass filter stage to process the monitored signals I_{DD} , while keeping the properties of the ramp test pattern. The filtering stage is not necessary for the CCO control output voltage V_{OSC} because in the loop filter a capacitance in parallel at the output absorbs the parasitic oscillations. The new test bench of the filtered VDD ramp test is shown in Figure 6.

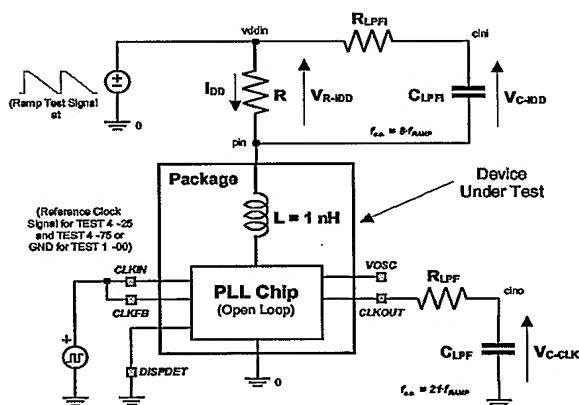


Figure 6. Quasi static testing setup with filter included

A normalized resistor of 1Ω is inserted in the power supply branch by means of which the power supply current is converted and measured as a voltage. A 1st order RC circuit is implemented as a low-pass filter to remove the ripple at a cut-off frequency 8 times higher than the ramp test frequency. This cut-off frequency is good enough for removing the ripples and extra distortions from the monitored I_{DD} signal. From, it is evident now that the test measurements are easier due to the clean waveforms. Special attention can be paid to the I_{DD} current signatures in case of RCTEST 4-75, which shows that the spikes due to the clock edges are mostly cleaned as well.

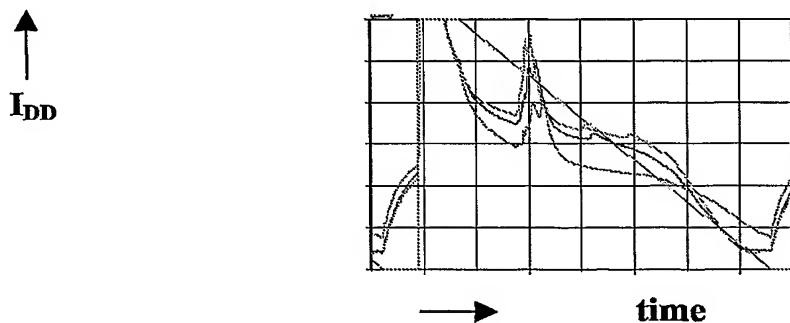


Figure 7. Filtered current signature

7. Fault Coverage Analysis

5 An inductive fault analysis was applied to the PLL to extract from the layout a realistic set of faults. The golden or fault-free simulation was performed with the use of an analog circuit simulator. This is the start of the entire fault simulation. The results of the golden simulation are used as a reference. At this stage the faults are introduced and simulated sequentially. The faults causing bridges are modelled as resistors between two nets. The results of the fault simulation are stored in a database and compared with the golden simulation. The detected and undetected faults can be determined by providing test limits to the database. The undetected faults are subject of further research. The simulations have been done in Dotss (Defect Oriented Test Simulation System), which is a Philips proprietary environment for fault simulation, and optimization.

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15 The layout extraction generated a ranked faultlist containing 680 bridges. Figure 8 shows the I_{DD} current signatures for the first 10 ones with reference to the TEST 1-00, TEST 4-25, and TEST 4-75.

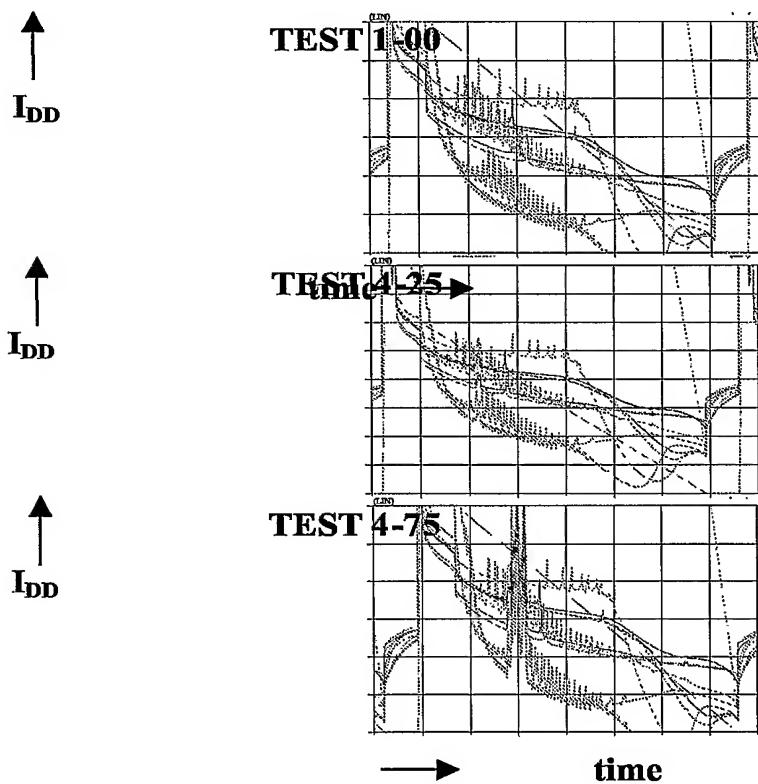


Figure 8. Example of faulty current signatures

20 Actually, these figures illustrate the potential of the method. Several signatures are completely different from the golden one. Some others signatures present values that are comparable to the golden's or are contained within the process limits in a certain period of time, but that have entirely different values in another one. This is especially achieved close to the rising edge of the test pattern. Indeed in this region the sampling points are fixed to check the PLL's output signals.

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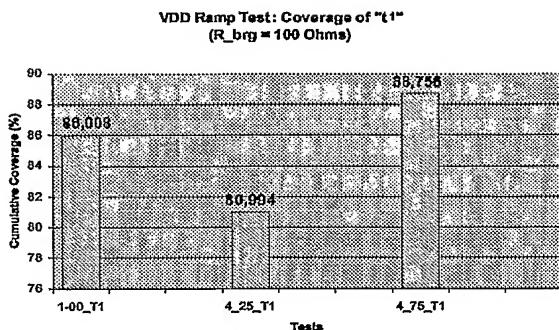


Figure 9. Projected fault coverages

Figure 9 and Figure 10 sum up the obtained results concerning the cumulative fault coverage of the three main tests with reference to the sampling points t_1 (zero crossing of current signature), on which the signals I_{DD} and VOSC are checked. Both the TEST 1-00 and TEST 4-75 give a very high coverage respectively of 86.008% and 88.756% for the test point t_1 . We conclude that the TEST 4-75 is the more effective for the highest fault coverage 88.756%. It is also possible to make it easier just testing the I_{DD} current on t_1 . In such case weighted fault coverage of 87.523% results. Anyway, also the TEST 1-00 (sampling only on t_1) can be considered a good one for the high fault coverage (86.008%), but mainly for the easy implementation based just on grounding the PLL's input CLKIN and CLKFB (in open-loop mode).

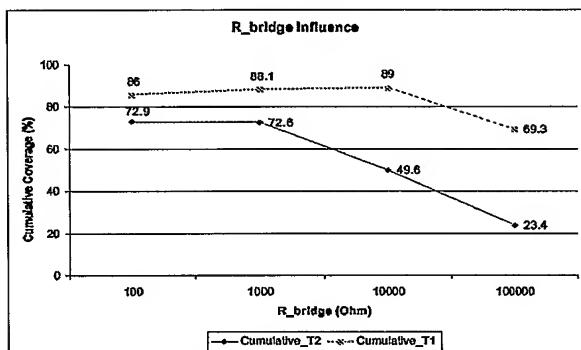


Figure 10. Projected fault coverage for resistive bridges

8. Experimental Results

We tested this methodology in the lab on the actual PLL. In this measurement setup the power supply pin is loaded with a capacitor of 300pF accounting for loading effects of the loadboard. A series resistor of 100 ohms is included between the power supply source and the PLL power pin, and a TEST -00 strategy was used. This resistor basically works as an I-V converter. Given the capacitive high loading of the loadboard the waveform has a period of 1us and a plateau of less than 250ns. The test equipment used is the following: Oscilloscope LeCroy LT364L (1GS/s), Active Differential Probe AP033 500 MHz, Agilent Arbitrary Waveform Generator 33250A (80 MHz), SMART PCF7961V0A in DIL28 package.

25 After a test optimization procedure we found the results shown in Table 1. Basically, measurements at only one or two sampling points are needed to test the circuit using this method. The test can be done in voltage mode without having to resort to long test times by I_{DDQ} testing. A digital tester with digitizer could be used to do this check.

30 Measurements were performed on only four ICs from one wafer, whereby deviations of 10 mV were observed at sampling point t1. All four parts are proofed to work correctly. The spread over multiple batches must be assumed significantly greater.

Table 1. Simulation results

Test Time	Test Value	Tolerance	FC
t1	-2mV	$\pm 2\text{mV}$	82.5%
1.9us	-2mV	$\pm 2\text{mV}$	83.6%
t1	-2mV	$\pm 10\text{mV}$	67.0%
2.6us	-2mV	$\pm 10\text{mV}$	67.3%

Figures 11-13 show measurements results of the VDD ramp method applied on (a) sample device(s). All signatures are averaged.

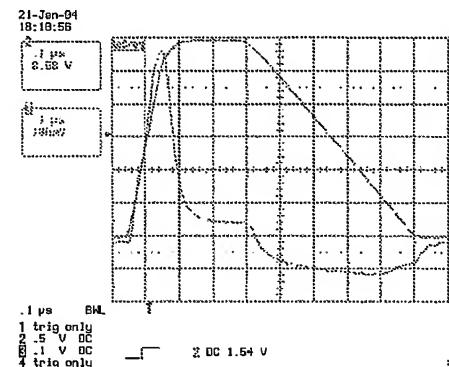


Figure 11. Measured signature. Traces correspond to power supply and to voltage drop across the power pin resistor.

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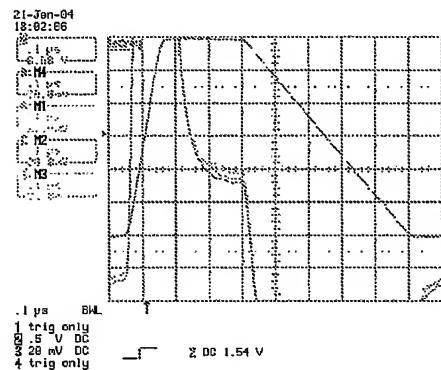
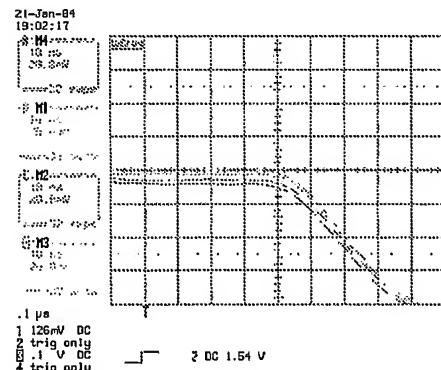


Figure 12. Measured signature of four IC samples



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Figure 13. Zoom in of Fig. 12

8. Conclusions

Future work could be performed to improve the performance of both the VDD ramp testing methods. This could be achieved by investigating the impact of the test pattern parameters (VDD ramp signal) on the monitored signals, with special attention to the effect on the slow and fast processes that constitute the worst condition for a chip in a wafer. Indeed, the process corners are a key factor in the proposed test approaches, because taken as limits to evaluate faulty signature and detect presence of faults in a chip. The proposed technique has been

5 tested in the lab and is not yet ready for production. In an engineering phase the calibration requirements could be demanding, for instance, high precision equipment was necessary to digitize the current signatures so as to localize the triggering time interval for the digitizer. Once the triggering point is identified, to be able to carry out the measurements around t1 it would be necessary to digitize with a speed between 30M and 50Msamples/s.

10 while our target for production testing is to use ATE with capabilities below 5Msamples/s. To account for test limits, precharacterization of engineering lots are needed. We observed a deviation of 10mV in the few samples we measured that could widen even more if more samples are considered. Nevertheless, an expected fault coverage of 67% can be attained using a tolerance window of 20mV range (+/-10mV). Further investigation is needed to understand the reliability, repeatability and accuracy properties of the approach for production testing.

10 The current calibration engineering phase is important as it characterizes and helps us understand the properties and constraints of the test approach.

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APPENDIX II

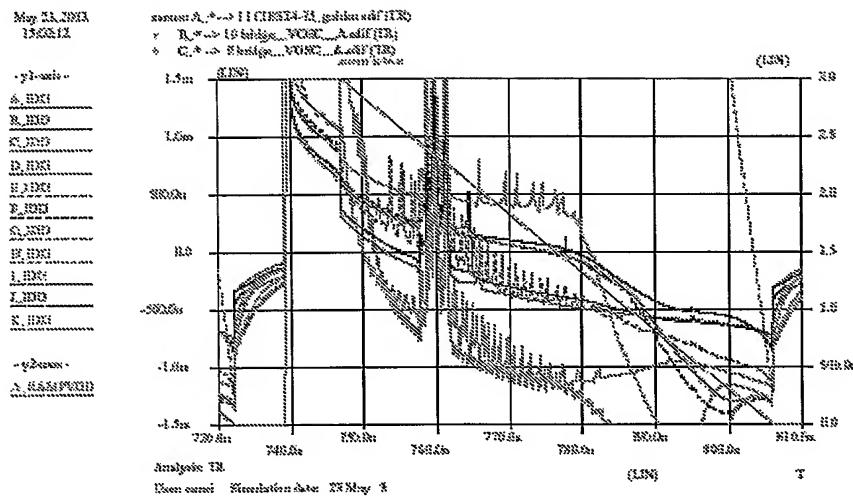


Figure 1a Typically faulty current signatures

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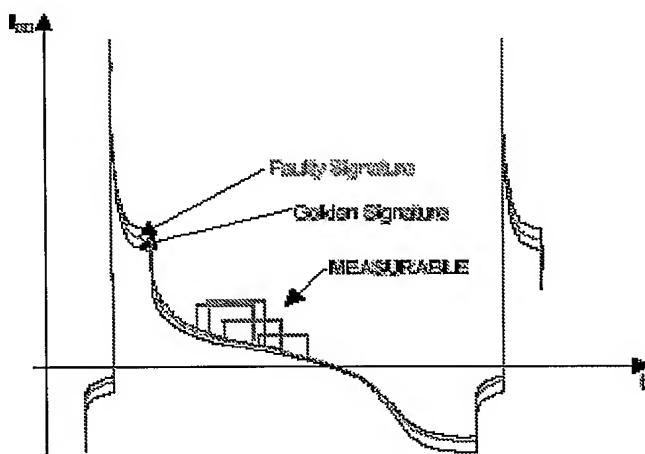


Figure 1b The exponential decay including undesired ripples

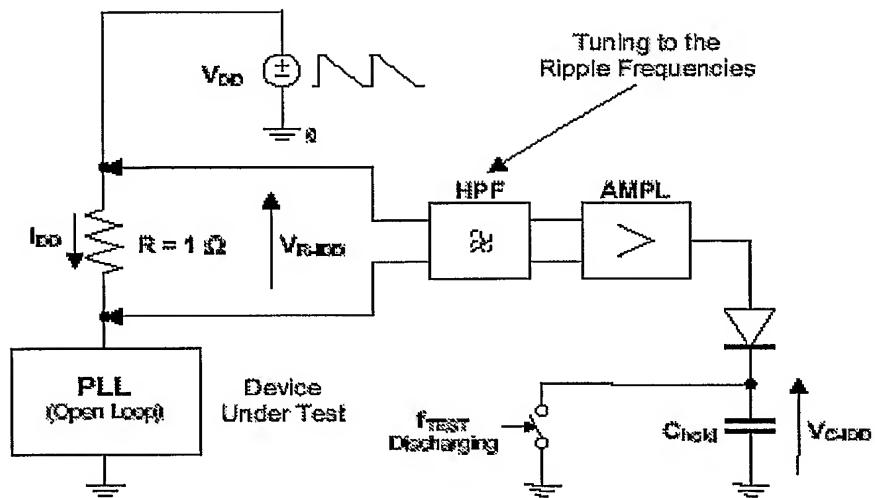


Figure 2. Basic block diagram of the BIST unit

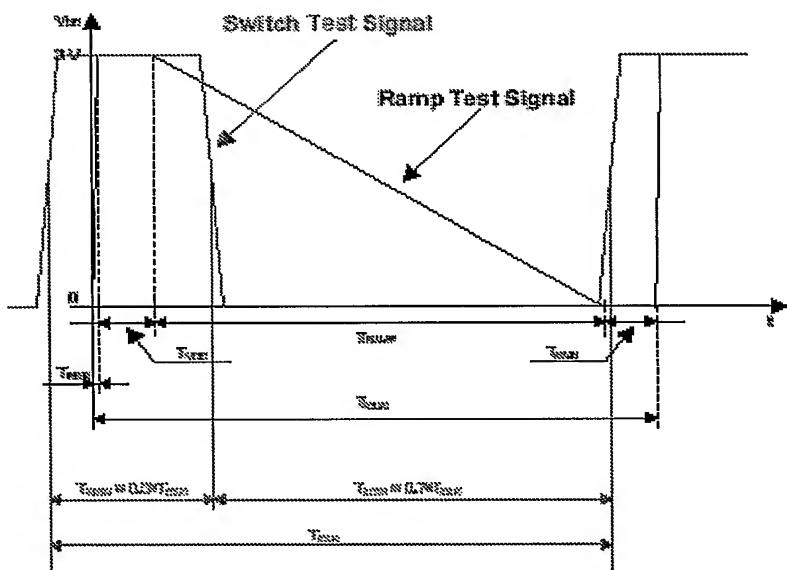


Figure 3. Power supply waveform and BIST switch waveform for signal sampling

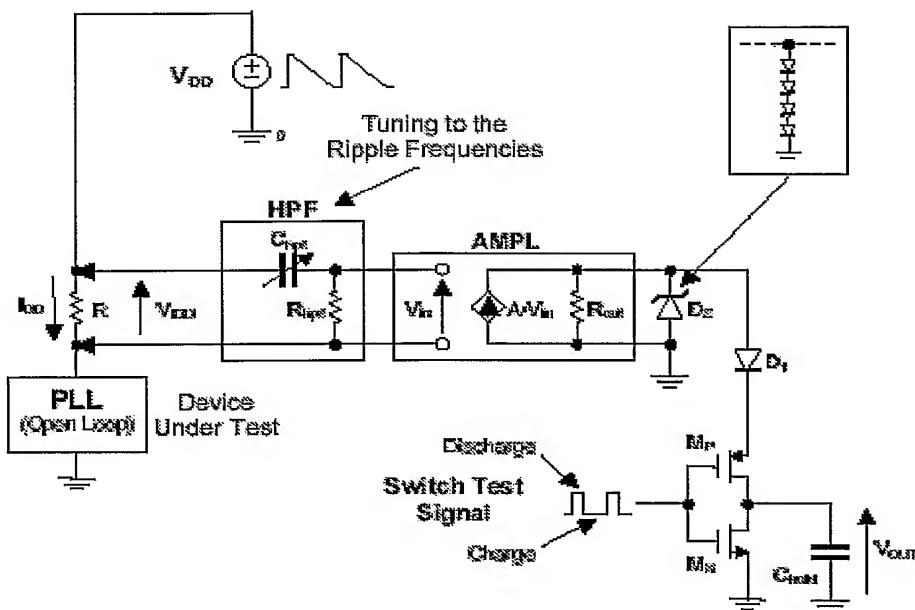


Figure 4. A more detailed implementation of the BIST

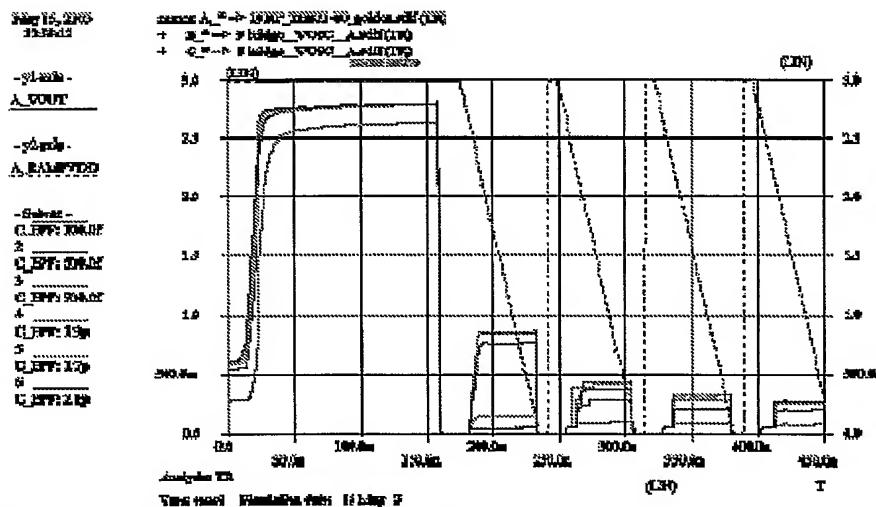


Figure 5. Power supply waveform and output of BIST for various capacitor values in the high-pass filter

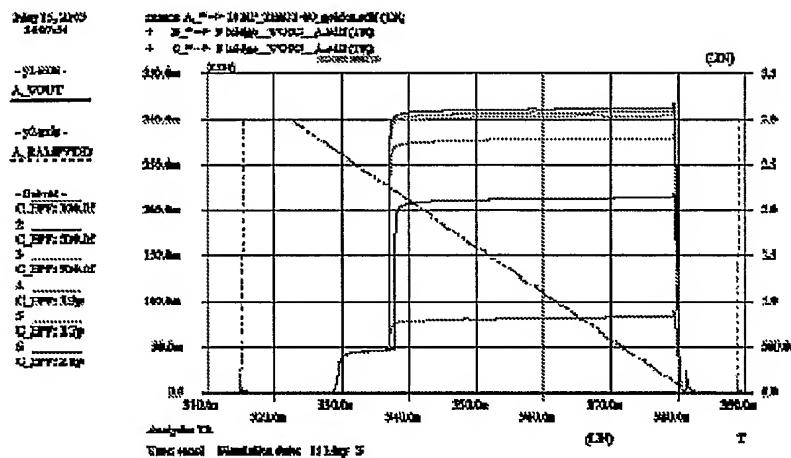


Figure 6. A zoom-in on the output signals of the BIST for various capacitor values of the high-pass filter.

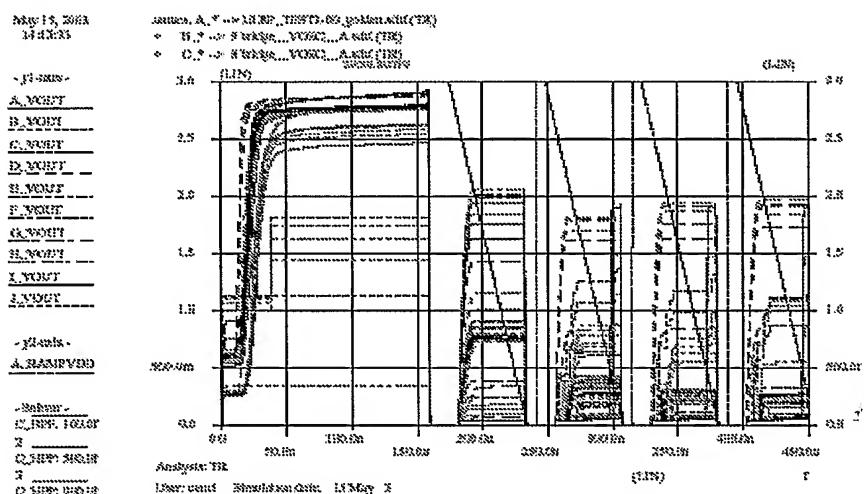


Figure 7. Example of output of BIST for a set of arbitrary bridges and for three different corner frequencies of the high pass filter.

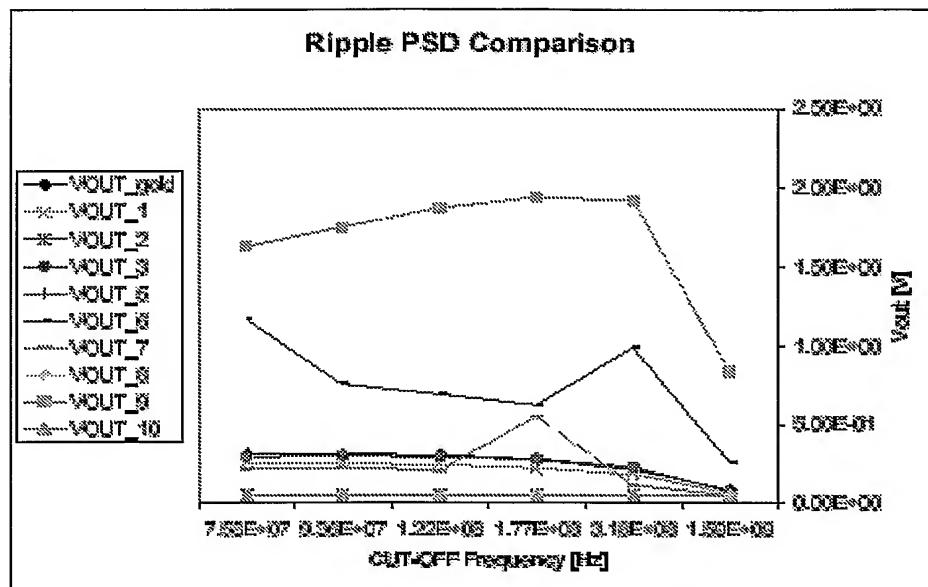


Figure 8. Using the output of the BIST for fault testing by power spectrum analysis

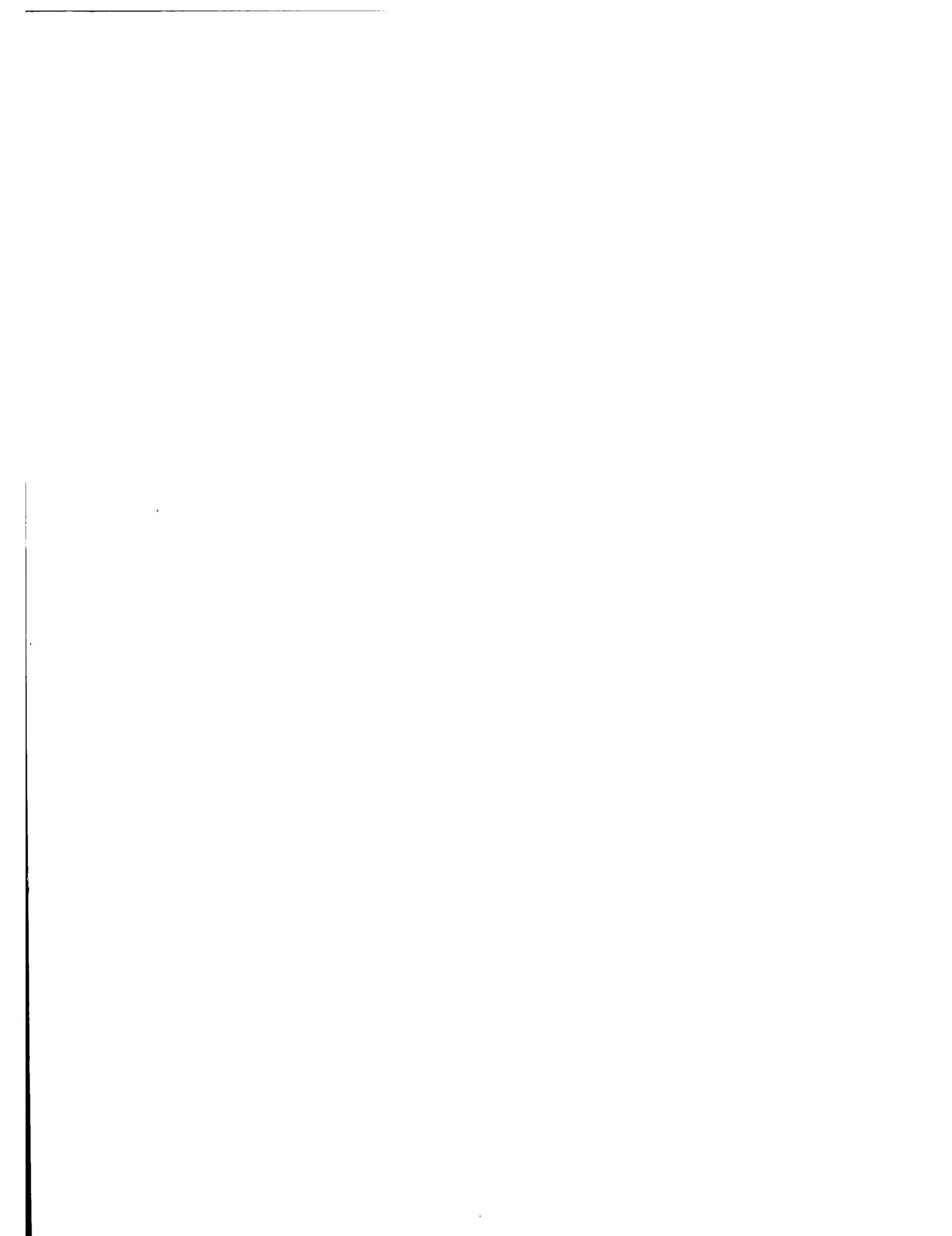
CLAIMS:

1. Method of testing a PLL comprising a phase detector for detecting a phase difference between an reference signal and a further signal, a filter for generating a control signal in response to a difference signal provided by the phase detector, and a controlled oscillator controlled by the control signal, according to which test method the PLL is driven in open loop mode, and is provided with a power supply voltage having a voltage variation profile, the voltage variation profile including a relatively fast voltage rise and a relatively slow voltage decay, and wherein an output signal of the PLL is compared with a template response.
5
- 10 2. Method according to claim 1, wherein the power supply voltage is maintained at a relatively constant value after the voltage rise and before the voltage decay.
- 15 3. Method according to one of the claims 1 to 3, wherein the voltage variation profile is periodically repeated
- 15 4. Method according to claim 1, wherein the repetition frequency is within the nominal operating frequency range of the PLL.
- 20 5. Method according to claim 3 or 4, wherein a constant signal value is provided as the reference signal and the further signal.
- 25 6. Method according to claim 3 or 4, wherein a periodic signal having the same frequency is provided as the reference signal and the further signal
- 25 7. Method according to claim 6, wherein the periodically repeated voltage variation profile lags with a phase difference of $\pi/2$ with respect to the periodic signal.
- 30 8. Method according to claim 6 wherein the periodically repeated voltage variation profile lags with a phase difference of $3\pi/2$ with respect to the periodic signal.
- 30 9. A method according to one of the previous claims, wherein the output signal is filtered, rectified and integrated.
- 35 10. A module including a PLL, the PLL comprising a phase detector for detecting a phase difference between a reference signal and a further signal, a filter for generating a control signal in response to a difference signal provided by the phase detector, and a controlled oscillator controlled by the control signal, the module comprising a power supply unit for providing the PLL with a substantially constant voltage during a normal operating mode and for providing the PLL with a power supply voltage having a voltage variation profile in a test mode, the voltage variation profile including a relatively fast voltage rise and a relatively slow voltage decay, the PLL including a feedback facility for in a normal operating mode providing a further signal derived from an output signal of the controlled oscillator, the
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feedback facility being disabled during test mode, the module further comprising a comparison unit for comparing an output signal of the PLL with a template response.

11. A module according to claim 10, wherein the comparison unit comprises a high-pass filter for filtering the output signal, a rectifying element for rectifying the filtered output signal and an integrator for integrating the rectified filtered output signal.

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